Energy minimization in the speed scaling model

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Abstract—Energy use of computer communication systems has quickly become a vital design consideration. One effective method for reducing energy consumption is dynamic speed scaling, which adapts the processing speed to the current load. We study network optimization that considers energy minimization as an objective as an objective.Studies have shown that mechanisms such as speed scaling can significantly reduce the power consumption of telecommunication networks.The dynamic voltage and frequency scaling in CPUs is an example of adjusting a device's control variable to trade off power consumption and performance. This idea of energy optimization through speed control has been subsequently applied to other components of electronic systems such as disk drives and wireless transceivers.

A processor is equipped with variable clock frequencies (speedy) feature and is used to schedule a set of given jobs with deadlines. Each speed change involves time/energy overhead and also impacts negatively the processors lifetime reliability. Based on above facts, problem of "energy aware scheduling, considering the number of speed changes and cost associated due to number of speed changes" is studied. Designing speed schedules to satisfy all jobs deadline and at the same time optimize the energy consumption and total cost involved due to speed changes. We develop algorithms that work close to the optimal and analyze its time complexities.

Index terms: dynamic voltage scaling, energy management, real time scheduling, speed scaling.

I. INTRODUCTION

POWERmanagement is increasingly important in computer communication systems. Not only is the energy consumption of the internet becoming a significant fraction of the energy consumption of developed countries, but cooling is also becoming a major concern. Consequently, there is an important tradeoff in modern system design between reducing energy use and maintaining good performance.

There is an extensive literature on power management, reviewed in [2] and [4]. A common technique, which is the focus of the current paper, is dynamic speed scaling. This dynamically reduces the processing speed at times of low workload, since processing more slowly uses less energy per operation. This methodology is adopted in many chip designs. Now days, speed scaling has been proposed for many network devices, such as switch fabrics [11], OFDM modulation clocks, etc. Energy management remains an important problem for computer systems, and in particular, for real time embedded systems. Here the target is to design and analyse algorithms for maximizing energy usage efficiency with the consideration of system performance requirements.

The rapid advance of processor design technology provides fast computing. Now a days processors like Intel SpeedStep and AMD PowerNOW, have been equipped with a feature to vary the clock frequency dynamically. The operating system is able to adjust the processor's clock frequency (speed) on the fly along with the supply voltage to execute jobs and reduce consumption at lower speeds. This functionality is called speed scaling and also dynamicvoltage scaling. Speed scaling is expected to satisfy some quality of service measures as well as to reduce overall energy cost, by manipulating modern processors' multiple speeds. Under the speed f (t) at time t, the processor consumes energy e(f(t)) per unit time and the function e(.) is assumed to be convex. The objective is to construct a schedule satisfying all jobs' deadline constraints and to minimize the total energy consumption, which is defined as $\int e(f(t))dt$.

Existing studies considered energy minimization through speed scaling without much attention to the impact of speed changes. Such changes typically involve time and energy overhead. Moreover recent studies indicate that the lifetime reliability of a CMOS circuit is directly related to the number and span of speed changes.

Hardware failures, such as cracks and fatigue failures are created not by sustained high temperatures but by the repeated heating and cooling of sections of the processor. This phenomenon is called as thermal cycling.

Using MTTF (Mean Time To Failure) to describe the expected processors life, the following Coffin Manson formula is used to characterize a processor's lifetime reliability:

$$MTTF \propto \frac{1}{c_0 \left(\Delta T_{mp} - \Delta T_0\right) q_x}$$

(1)

Where C_0 is a material dependent constant ΔT_{mp} is the entire temperature cycle range of the device ΔT_o is the portion

of the temperature range in the elastic region, q is the coffin mason exponent, and x is frequency (number of occurences per unit time) of thermal cycles.

Above equation clearly indicates that an algorithm which

frequently changes the processors speed results in large x and ΔTmp . Thus a schedule that frequently changes speed may result in large temperature cycle range and therefore affect the processor's life time reliability adversely. Simulations have confirmed that various speed scaling energy aware policies have different impacts on processor's reliability in terms of MTTF. The number of speed changes(x in equation 1) is a critical factor in determining a processor's reliability under the thermal cycling phenomenon.

The main purpose is to undertake a theoretical investigation of speed scaling algorithms by considering the cost and number of speed changes. The results remain valid for arbitrary convex energy consumption functions $e(\cdot)$ with e(0)=0. The requirement is not that $e(\cdot)$ should be some closed function form; it may be given by various closed formulas in different frequency ranges. In this paper, we assume that only the CPU's clock frequency can be adjusted.

II. MODELS AND PROBLEM DEFINITION

We consider a single processor setting. The processor has variable clock frequencies (speeds).Under a speed f, the processor consumes energy e(f) per unit time and assume that the function $e(\cdot)$ is convex and e(0)=0. We note that in scaling speeds, the processor's frequency and supply voltage are both adjusted(dynamic voltage/frequency scaling). Hence, in rest of the paper we will understand that frequency/speed changes always involve the corresponding voltage change.

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Consider a set of *n* real time jobs $J = \{J_1, J_2, \dots, J_n\}$.Each job J_i has a release time $r_i \in R^+$, a processing time(also called as worst execution time), $p_i \in R^+$, and a deadline $d_i \in R^+$. Under the speed f, it takes time pi/f to complete the job J_i . Considering the pre-emptive scheduling and assuming the cost of pre-emption is negligible.

The objective in this study is to design scheduling algorithms to finish all the jobs before their deadlines by considering the objectives of minimizing the energy consumption, as well as the number and cost of speed changes.

Definition 1 (Speed schedule): A speed schedule can be viewed as piecewise constant curve, specifying the speed the processor employs in each time interval. Assume that the CPU changes speed m times during the execution. Then the speed

each of these intervals. Let the *m time* intervals be: I₁:=(t_0 , t_1], I₂:=(t_1 , t_2],..., I_m:= (t_{m-1} , t_m].

The triple(t_{i-1} , t_i , s_i) corresponds to the *i*th time interval $I_i = (t_{i-1}, t_i)$ (0<*i*<m and $t_0 = 0$) in which the processor runs at a speed $s_i \ge 0$. Hence the speed scheduler Ψ is specified by m triples:

 $\Psi: \{(t_0, t_1, s_1), (t_1, t_2, s_2), \dots, (t_{m-1}, t_m, s_m)\}$

Figure below illustrates an example schedule. The schedule employs 4 distinct speeds f_1 , f_2 , f_3 , f_4 in 6 time intervals, where $s_1=s_4=f_1$, $s_2=s_6=f_4$, $s_3=f_2$, and $s_5=f_3$.

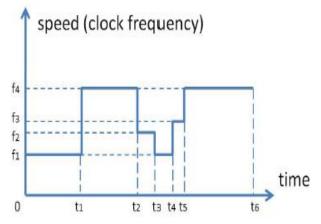


Figure 1.A piecewise curve describing the time intervals and the processor's speed in each interval.

We can call t_i a *speed switching point*. Without loss of generality, we can assume that the processor is in *idle* state initially at time 0 ($s_0 = 0$) and gets back to the idle state after processing all the jobs ($s_{m+1} = 0$). Thus a schedule with m time intervals have m+1 speed switching pointst₀, t_1 , t_2 , ..., t_m .

The total energy consumption of such a schedule is calculated as:

 $\mathbf{E}^{\Psi} = \sum_{i=1}^{m} e(s_i)(t_i - t_{i-1})$ For the example in figure:

$$\begin{split} E^{\Psi} &= e(f_1) \ (t_1 - 0) + e(f_4) \ (t_2 - t_1) + e(f_2) \ (t_3 - t_2) + e(f_1) \ (t_4 - t_3) \\ &+ e(f_3) \ (t_5 - t_4) + e(f_4)(t_6 - t_5) \\ &= e \ (f_1) \ (t_1 + t_4 - t_3) + e \ (f_4) \ (t_2 - t_1 + t_6 - t_5) + e \ (f_2) \ (t_3 - t_2) + \\ &e \ (f_3) \ (t_5 - t_4). \end{split}$$

To incorporate the penalty of changing clock frequencies, consider that each speed change from the frequency s_i (in interval I_i) to the frequency s_{i+1} (in the interval I_{i+1}) involves a cost $c_{i,i+1} \boldsymbol{\epsilon} \ R^+$ ($c_{i,i+1} \ may$, for example ,reflect the speed change's negative impact on the processor's lifetime reliability).

Assuming that the cost of a speed change is a convex function of the difference between the previous and the new speed values .For instance, switching from f_4 to f_1 may be more costly than switching from f_4 to f_3 , if $f_1 < f_3 < f_4$. Consequently, the function $c(\cdot)$ is convex and $c_{i,i+1}$ is the value

of $c(\cdot)$ for $|s_i - s_{i+1}|$.

 $c_{i,i+1} := c(|s_i - s_{i+1}|)$, where $s_o = s_{m+1} = 0$ (2)

We now present the formulation of two optimization problems.

Problem1: Minimizing sum of energy consumption and costs associated due to speed changes.

Let E^{Ψ} denote the total energy consumed by the schedule Ψ to complete the set of jobs **J** by their deadlines. Assume Ψ has m time intervals. The total cost associated with all the clock speed changes during this schedule is $\sum_{i=0}^{m} c_{i,i+1}$ where s0 and s_{m+1} are defined as 0(assumed above). In this problem, the aim is to minimize $E^{\Psi} + \beta \sum_{i=0}^{m} c_{i,i+1}$, where β is a given constant. After normalizing $c_{i,i+1}$, we can remove β and formulate the problem as

 $\operatorname{Min.}(\sum_{i=1}^{m} e(s_i)(t_i - t_{i-1}) + \sum_{i=0}^{m} c'_{i,i+1}),$

where $s_0 = sm+1 = 0$ and $c'_{i,i+1} = c_{i,i+1}/\beta$.

Problem2: Minimizing sum of energy consumption under a fixed number of speed changes.

Let E^{Ψ} and m denote the total energy consumed and the total no of speed changes in the schedule Ψ to complete the jobs in Jby their deadlines, respectively. Let M be the upper bound on the number of speed changes. The objective is to minimize E^{Ψ} subject to m $\leq M$. That is,

Min $\sum_{i=1}^{m} e(s_i)(t_{i-1})$, subject to $m \le M$.

Problem2 considers the number of speed changes as a constraint.

III. ALGORITHMS AND ANALYSIS

In the following, we present algorithmic solutions for the two problems discussed above. We analyse their performance as well.

The algorithms have no restrictions over the number of processor's speed changes. The models discussed above have their own algorithmic challenges.

A. The formulation for minimizing sum of energy consumption and costs incurred due to speed changes is discussed here.

Assuming that the schedule Ψ has m time intervals $I_i = (t_{i-1}, t_i] (1 \leq m)$ and within each interval I_i , the processor keeps running at constant speed $s_i \geq 0$. The system does not consume any energy after finishing the last job.

The objective is

$$\operatorname{Min}(\sum_{i=1}^{m} e(s_i)(t_i - t_{i-1}) + \sum_{i=0}^{m} c_{i,i+1})$$
(3)

where $c_{i,i+1}$ is scaled by a factor β from its definition as discussed before.

Defining OPT as an optimal algorithm minimizing the sum of energy consumption and the costs incurred due to speed changes. The job is to determine all the candidate values that ti in above equation (3) can take place. The function c(.) is assumed to be convex function, hence determining the optimal schedule's speed switching points heavily depends on the function c(.) itself.

It is possible that the processor will need to change its speed in each time slot to optimize equation(3).Instead of designing algorithm for some specific functions c(.), a large class of algorithms called *event driven* DVS (dynamic voltage scaling) is discussed. The purpose of introducing an event driven DVS algorithm for the problem is to show that there exists an optimal convex programming based solution, and this solution's framework can be proved to generate optimal solutions for other future problems.

Event Driven DVS Algorithms: For event driven DVS algorithms, speed changes (speed switching points) only happen at jobs' release times and /or deadlines.

Event Driven DVS algorithms have the distinct advantage of keeping the run time overhead due to DVS low, as opposed to DVS algorithms that requires speed change at arbitrary points during execution :The CPU scheduler , That is invoked at task release times and deadlines , can also regulate the frequency according to the pre- determined speed schedule during the same invocation . As a result, the optimality of event driven DVS algorithms will prove very useful in practice.

Let $\mathbf{J} = \{J_1, J_2, \dots, J_n\}$ denote the n jobs to be scheduled. A job Jj is represented by a triple (r_i, d_i, p_i) .

Let $R = \{r_1, r_2,, r_n\}$, 1	$\{n_n\}$ and
$D = \{d_1, d_2, \dots, d_n\}$	\mathbf{l}_n }.	

Let Z=R U D to denote the union of all the release times and deadlines of jobs .Note that $|Z|=|R U D| \le |R| + |D| \le 2n$. Sort all the values in Z in increasing order and index them as $z_1, z_2, \ldots, z_{n'}$, where $n' \le 2n$. Without loss of generality, assume $z_1 = 0$. Before the last deadline $z_{n'}$, the time range is divided into n' - 1 non overlapping intervals ($z_i, z_{i+1}]$, V $1 \le I \le n' - 1$. We name the interval $T_{i,i'} := (z_i, z_i']$ as a scheduling interval. For each scheduling interval $T_{i,i'}$, compute its corresponding work load by a variable $W_{i,i'}$ and processing capacity as $P_{i,i'}$, given the speed s_i assumed for each interval $(z_{l-1}, z_l]$.

Pi,i'
$$= \frac{\sum_{j} p_{j}}{z_{i'-z_{i}}}$$
, where $z_{i} < r_{j} < d_{j} < z'_{i}$
Wi,i' $= \sum_{l=i+1}^{i'} s'_{l}$, $i < l < i'$

Where s_l ' is the speed variable to denote at which speed the processor runs in the interval $(z_{l-1}, z_l]$. In order to complete all the jobs by their deadlines, the processing capacity should be at least the workload requirement for each time interval.

The remaining task is to determine s'_1 such that all the jobs in J can be finished by their deadlines and the objective

$$\sum_{l=2}^{|z|} e(s_l') (z_l - z_{l-1}) + \sum_{l=2}^{|z|+1} c(|s_l' - s_{l-1}'|) \text{ is minimized.}$$

The problem is formulated using a convex program as below :

$$\begin{aligned} \min \sum_{l=2}^{|z|} e(s'_l) &(z_l - z_{l-1}) + \sum_{l=2}^{|z|+1} c(|s'_l - s'_{l-1}|) \\ \text{Subject to} \quad W_{i,i'} \geq P_{i,i'}, \forall \ 1 \leq i \leq |Z| \end{aligned}$$

Studied above, is the analysis of correctness and time complexity for the algorithm that computes an event-driven DVS schedule for the problem.

For a given set of real time jobs with known processing times, pre-emptive EDF is optimal in the sense that any feasible job set can be also scheduled in a feasible manner by the EDF policy.

ALGORITHM

- 1. Let $J = \{ J_1, J_2, \dots, J_n \}$; i.e. 'n' jobs to be scheduled.
- 2. $J_j = \{ r_j, d_j, p_j \}$; where 'j' is any general term for (1, 2,...,n) i.e. in between 1 and n.
- 3. R= { $r_1, r_2, \dots, r_j, \dots, r_n$ } and D={ $d_1, d_2, \dots, d_j, \dots, d_n$ }
- 4. Z = RUD
- 5. As there are n values in r and n values in d, hence, $IZI \le IRUDI \le IRI \ UIDI \le 2n$
- 6. Sorting in increasing order i.e. $z_1, z_2, \ldots, z_{n'}$, where $n' \leq 2n$. As there is union of two i.e. R and D, hence the values are doubled i.e. from (1 to 2n) or (1 to n') as $n' \leq 2n$.
- 7. Now divide these intervals into (n'-1) nonoverlapping intervals i.e. $(z_i, z_{i+1}), T_{i,i'} =$ scheduling interval.
- 8. There are at most " C_2 " scheduling intervals.
- 9. For each scheduling interval, we can calculate Pi,i' $=\frac{\sum_j p_j}{z_{i'}-z_i}$, where zi < rj < dj < zi'.[Processing capacity]

Wi,i' = $\sum_{l=i+1}^{i'} s'_l$, i < l < i'. [Workload]

10. Minimize the energy using the formula :

$$\operatorname{Min} \sum_{l=2}^{|z|} e(s_l') (z_l - z_{l-1}) + \sum_{l=2}^{|z|+1} c(|s_l' - s_{l-1}'|)$$

subject to $W_{i,i'} \ge P_{i,i'}, \forall 1 \le i \le |Z|$

11. Repeat a schedule running jobs in order using different speeds $\{s'_i\}$.

B. Minimizing energy consumption under limited number of speed changes.

Assuming M be the upper limit on the number of speed changes that a speed schedule Ψ is allowed to schedule jobs, we present algorithm for the problem. Similar to the problem1 we sort all the values in Z in increasing order and index them as z_1, z_2, \ldots, z_n where $n' \leq 2n$. Thus, the whole time s_i divided

into n' – 1 non overlapping intervals (z_i , z_{i+1}] in which the processor runs possible positive speeds, $\forall 1 \leq I \leq n^2$ - 1. The

interval T_{i,i'} := ($z_i, z_{i'}$] (i' \geq i+1) is a scheduling interval. There are at most $\binom{n'}{2} = \frac{n'(n'-1)}{2}$ such scheduling intervals. For each scheduling interval T_{i,i'}, we can calculate its corresponding workload W_{i,i'}, and its processing capacity Pi,i' as earlier, given the speeds'l assumed for each interval (z_{1-1}, z_1].

The remaining task is to determine s'_1 such that all the jobs in J can be finished by their deadlines and the objective is to bound the number of speed changes by M.

ALGORITHM

- 1. Let J = { J₁,J₂,...,J_n}; i.e. 'n' jobs to be scheduled.
 - 2. $J_j = \{ r_j, d_j, p_j \}$; where 'j' is any general term for $(1, 2, \dots, j, \dots, n)$ i.e. in between 1 and n.
 - 3. $R = \{ r_1, r_2, \dots, r_j, \dots, r_n \}$ and $D = \{ d_1, d_2, \dots, d_j, \dots, d_n \}$
 - 4. Z = RUD
 - 5. As there are n values in r and n values in d, hence, $IZI \le IRUDI \le IRI \ U \ IDI \ \le 2n$
 - 6. Sorting in increasing order i.e. $z_1, z_2, \ldots, z_{n'}$, where $n' \leq 2n$. As there is union of two i.e. R and D, hence the values are doubled i.e. from (1 to 2n) or (1 to n') as $n' \leq 2n$.
 - Now divide these intervals into (n'-1) nonoverlapping intervals i.e. (z_i, z_{i+1}), T_{i,i'} = scheduling interval.
 - 8. There are at most " C_2 " scheduling intervals.
 - 9. For each scheduling interval, we can calculate Pi,i' $= \frac{\sum_j p_j}{z_{i'} - z_i}$, where zi < rj < dj < zi'.[Processing capacity]

Wi,i' = $\sum_{l=i+1}^{i'} s'_{l}$, i < l < i'. [Workload]

10. Minimize the energy using the formula :

$$\operatorname{Min} \sum_{l=2}^{|z|} e(s_l') (z_l - z_{l-1})$$

subject to $W_{i,i'} \ge P_{i,i'}, \forall 1 \le i \le |Z|$

$$\sum_{l=2}^{|z|+1} c(|s_l' - s_{l-1}'|) \le \mathbf{M}$$

11. Repeat a schedule running jobs in order using different speeds $\{s'_l\}$

IV. SIMULATED RESULTS

The program asks for different values like, Processing Speed of processor, Release Times, Deadline Times. The data entered calculates different scheduling times, processing capacity, and the various speeds proportional to the scheduling times. The speed is indicated for each of the time segments. Finally the main subject is displayed i.e. energy consumption before optimization and energy consumption after optimization.

The results can be checked for various processors having different processing speeds and different timing instants.

Different Speed schedules according to the deadlines and the overall energy consumption is calculated with the help of this program.

For example:

Enter the speed value of the processor: 3000Hz First release time is always zero: Enter the first dead line which is more than zero: 8ms Enter the second release time: 14ms Enter the second dead line: 62ms Enter the third release time: 81ms Enter the third dead line: 105ms z = 0 8 14 62 81 105

 $t = 8 \quad 6 \quad 48 \quad 19 \quad 24$

p1 = 6 11 60 81 84

Processing Capacity will be 11.5965 Speed during First segment is 60.00Hz Speed during Second segment is 1260.00Hz Speed during Third segment is 870.00Hz Speed during Fourth segment is 150.00Hz Final energy after optimization is 71.30 Final energy before optimization is 78.00

V. CONCLUSION

Motivated by enhancing processor's lifetime reliability from the perspective of designing speed scaling algorithms, investigation is about energy-aware scheduling algorithms in this paper. Contributions include a scheduling algorithm for one model, optimizing energy consumption and cost of frequency changes. Convex Programming Technique is applied for general model. The algorithm that is provided is close to optimal.

VI. FUTURE WORK

In the future research, study of relationship between the frequency and the temperature/heat generated by the processor, in order to get a better understanding processor's lifetime reliability can be envisaged. By doing so a more precise model on processor's lifetime reliability and a good algorithm solution can be implemented.

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